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Design and Analysis of Energy Recovery Logic for Low Power Circuit Design

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ABSTRACT
In the past major concern of the VLSI designer were area, performance, cost and reliability. In recent years, however this has begin to change and increasingly power is being given comparable weight to area and speed considerations. There are numerous methods that can be used to reduce the power consumption of VLSI circuits. These can range from low level measure such as using a lower supply voltage or using high threshold voltage to high level measures such as clock-gating or power down modes. The one that motivated this investigation was energy recovery logic. In this paper, Efficient Charge Recovery Logic (ECRL), Modified Energy Recovery Logic (MERL), Positive-Feedback Adiabatic Logic (PFAL) and Advance Energy Recovery Logic (AERL) are studied in consideration to their power consumption. This logic is more power efficient as compared to traditional CMOS logic. Also an enhancement is proposed for existing energy recovery logic to provide more power efficient circuit.
Keywords – CMOS, ECRL, MERL, PFAL, AERL

I. INTRODUCTION

The power consumption of electronic device is increasing rapidly with the rise in operating frequency and performance of the devices. In recent years, there are an ever-increasing number of portable applications requiring low power and high throughput than ever before. Moreover, in case of the portable devices high performance, light weight, and long operation time are the major design consideration, which are again conflicting objectives. Designing low-power digital systems especially the fundamental blocks like adder, multipliers and oscillators etc are becoming equally important to designing a high performance system.

The energy recovery logics circuits offer considerable improvement in power consumption over static CMOS at low frequencies [1]. Energy recovering logic reuses charge and therefore consumes less power than non-energy recovery logics. An energy recovering logic charges the load capacitance during logic high to drive the gates rather than draining charge to ground [2][3][4]. In non energy recovering logic, the charge applied to the load capacitance during logic level high is drained to ground during logic level low.

Basic principal of energy recovery process is shown in figure 1. Charges are fed from the power supply, guided through PMOS transistor and then dumped into the ground terminal.
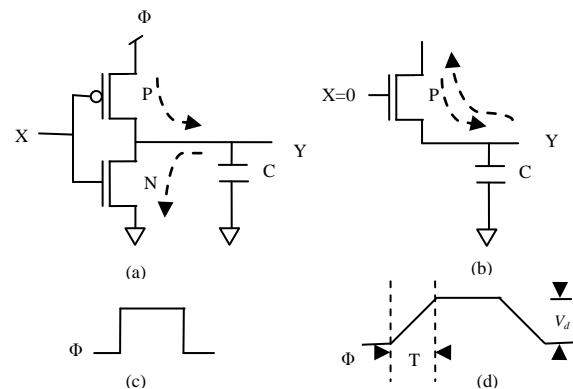

Figure 1: Conventional CMOS inverter and clocks

The amount of energy dissipated when charging capacitance 'C' from 0 to V_{dd} in time T with a linear power supply voltage is given as:

$$ — \qquad — \qquad — \tag{1} $$

Considering T >> RC energy dissipated is given as:

$$ — \tag{2} $$

When T << RC as in normal CMOS *RC* energy dissipated is given as:

$$\_ \qquad (3)$$

Clocked CMOS circuits with steadily rising and falling power-clock are expected to obtain a significant energy saving [5]. However, the operational constraint is that the output signal should track the power clock's gradually rising and falling behavior to accomplish the charging and discharging process increases difficulty in the circuit design. There are different architecture number of adiabatic logic architectures proposed such as efficient energy recovery logic (ECRL) 2N-2N2P logic and positive feedback adiabatic logic (PFAL) [6][7][8]. Each logic family has some advantage and disadvantage as well. Energy dissipation can be divided in two types of losses: one is adiabatic loss and other is non adiabatic loss. Adiabatic loss is generated due to switching resistance of the transistor when current flows through it. This type of loss is less because the switching resistance offered by the charging path is low as the functional block is in parallel with the charging MOS transistor.

The non adiabatic losses occur due to the threshold voltage of the transistor used in charging path. During the recovery phase, the energy is only partially recovered from the output load C_L. When the output voltage goes below the threshold voltage then the PMOS transistor goes in off condition and logic blocks further recovers the energy. During the evaluation phase, this uncovered charge gets dissipated as loss when the new input gets applicable.

This paper studies the different energy recovery logic families for power efficient circuit design. For this purpose three energy recovery logic families namely efficient charge recovery logic, modified efficient charge recovery logic and positive feedback adiabatic logic are taken for the present study. Also an advance energy recovery logic circuit is proposed with reduction in circuit complexity which further reduces power consumption.

II. ENERGY RECOVERY LOGIC CIRCUITS

2.1 Efficient Charge Recovery Logic (ECRL)

The schematic of the ECRL inverter [2] is shown in figure 2. An AC power supply Φ is used to recover and reuse the supplied energy. In ECRL logic precharge and evaluation are performed simultaneously. Full output swing is obtained because of cross coupled PMOS transistors both in the precharged and recovery phase. This circuit suffers from non adiabatic loss. This logic has the similar circuit arrangement as cascade voltage switch logic

(CVSL) with differential signaling [3]. It is assumed that signal 'In' is at high and signal 'Inbar' is at low level. At the beginning of a cycle, when the supply clock Φ rises from zero to V_{dd}, signal 'Out' remains at a ground level, because 'In' signal turns ON the transistor MN2 and 'Outbar' follows Φ through MP1. When Φ reaches V_{dd} the outputs hold valid logic levels. These values are maintained during the hold phase and are used as inputs for evaluation of the next stage. After the hold phase, Φ falls down to a ground level and 'Outbar' node returns its energy to Φ so that the delivered charge is recovered. Thus, the clock Φ acts as both a clock and power supply. Wait phase is inserted for clock symmetry. In this phase, valid inputs are being prepared in the previous stage.
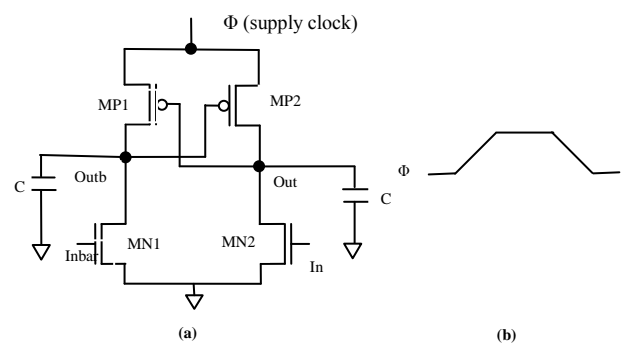

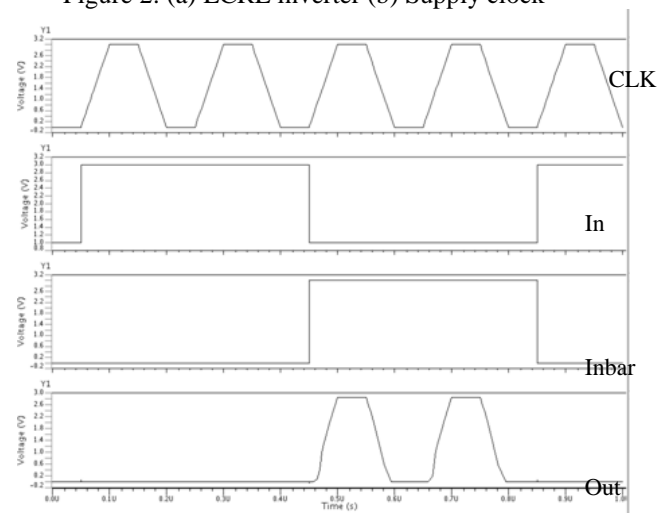Figure 2: (a) ECRL inverter (b) Supply clock

Figure 3: ECRL inverter output waveform

Figure 3 shows the simulated results for ECRL inverter with SPICE in 0.5μm CMOS technology. In ECRL the peak value of the supply clocks are all set to 3V, the load capacitances are set to 20fF and the frequency of the power clock are set to 5MHz.

2.2. Modified Energy Recovery Logic (MERL)

The schematic of the modified energy recovery logic circuit (MERL) inverter and the supply clocks are

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shown in Figure 4(a) and (b) respectively. The biggest difference between ECRL and MERL is that the energy can be completely recovered in the recovery phase in the MERL circuit. Figure 5 shows the simulated results of modified ECRL with SPICE in 0.5μm CMOS technology.
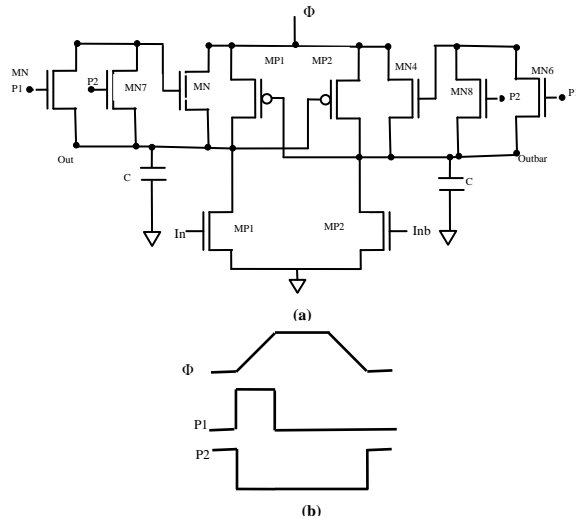

(a)

(b)

Figure 4: (a) Schematic of the MERL inverter
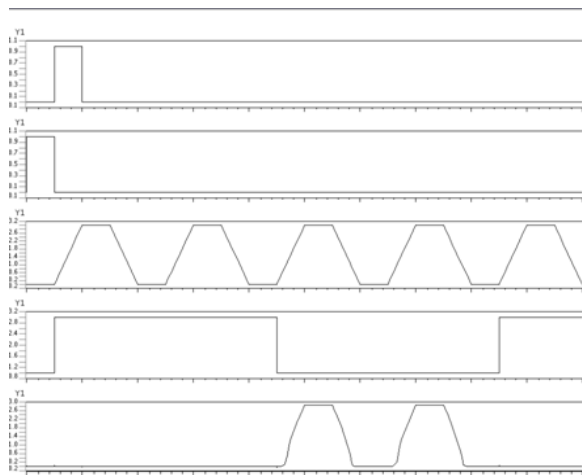(b) Supply clocks

Figure 5: MERL output waveform

2. 3 Positive-Feedback Adiabatic Logic (PFAL)
The structure of PFAL logic is shown in Figure 6. It uses a cross coupled latch of two PMOS transistor and two NMOS transistors instead of two PMOS transistors as in case of ECRL. Two n-trees realize the logic functions. This logic family also generates both positive and negative outputs. The two major differences with respect to ECRL are that the latch is made by two pMOSFETs and two nMOSFETs, rather than by only two pMOSFETs as in ECRL, and that

the functional blocks are in parallel with the transmission pMOSFETs. Thus the equivalent resistance is smaller when the capacitance needs to be charged. During the recovery phase, the loaded capacitance gives back energy to the power supply and the supplied energy decreases. This logic is more power efficient as compared to earlier logics. Figure 7 shows the simulated results of PFAL inverter in SPICE in 0.5μm CMOS technology.
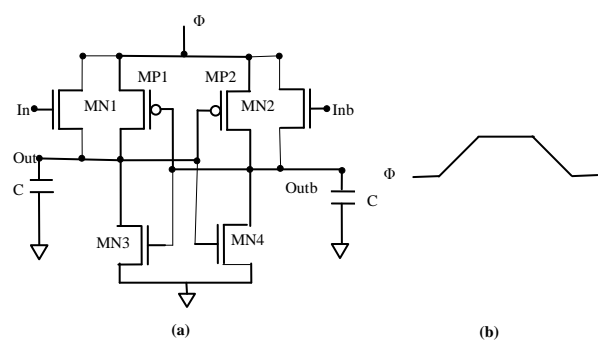

(a)   **(b)**

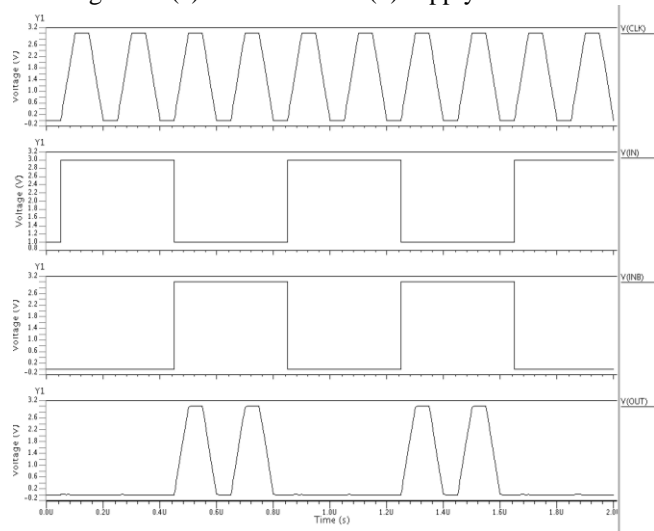Figure 6: (a) PFAL inverter (b) supply clock

Figure 7: PFAL inverter output waveform

II. PROPOSED ADVANCE ENERGY RECOVERY LOGIC Circuit (AERL)

The structure of AERL is shown in figure 8. Various Energy Recovery Circuit (ERCs) towards adiabatic circuitry for ultra low implementation require two conducting paths for charging and discharging of load capacitor. But only one path is conducting at any instant of time. So design of the circuit is more complex and it also increases the delay and energy consumption. In proposed energy recovery logic circuit, there exist same path for charging and discharging of load capacitor and as a result, the

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circuit complexity is reduced. The schematic of the proposed energy recovery logic inverter is shown in figure 8 (a). The clock used for this design is shown in figure 8 (b)
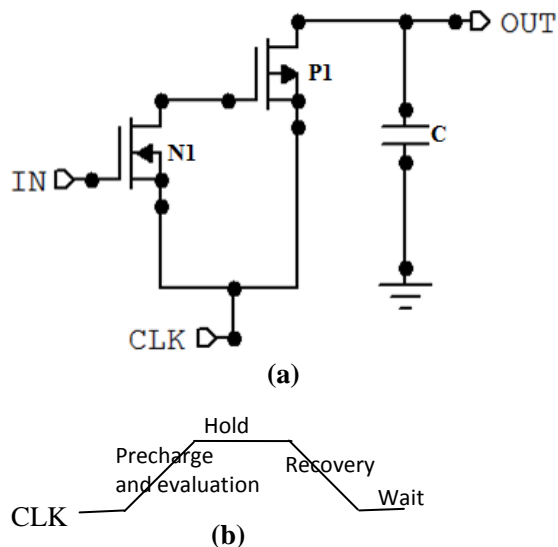
.

(a)

(b)

Figure 8: (a) Proposed Advance ERL Inverter (b) Supply Clock

Let us assume IN is at high i.e. logic "1" and capacitor is initially uncharged. When IN is high N1 transistor is *on* and gate terminal of transistor P1 is connected to source as shown in Figure 9. So M1 transistor is equivalent to *diode*. Any change in CLK value does not impact the OUT node which is still at low voltage because diode is in reverse mode and any charge does not accumulate at capacitor C as shown in Figure 9. Hence it behaves like open circuit. So OUT is low i.e. logic "0".
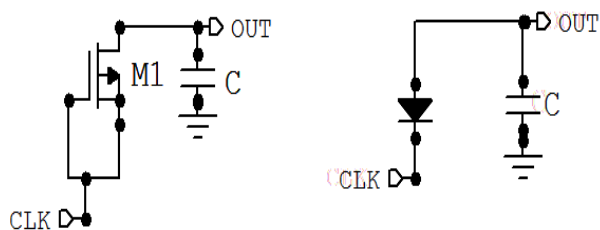

Figure 9: Equivalent Circuit of Proposed ERL Inverter when value of IN is high

Now let us assume IN is at low i.e. logic "0". When IN is at low then N1 transistor is *off* and P1 transistor is on as shown in figure 10. OUT node follows the CL and thus, the CLK acts as both a clock and power supply. The output of ERL inverter is shown in figure 11.
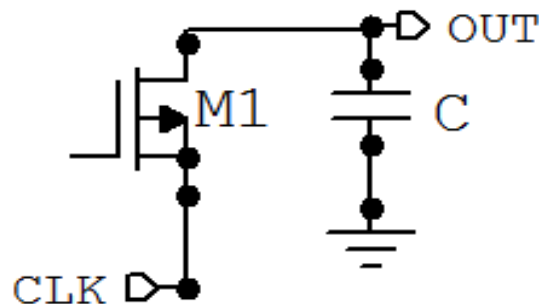

Figure 10: Equivalent Circuit of Proposed ERL Inverter when value of IN is low
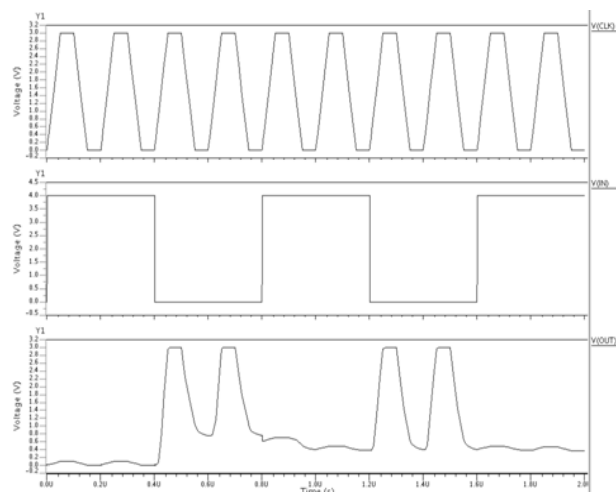

Figure 11: Clock, Inputs and Output waveform of Proposed ERL Inverter

3.1 Proposed ERL Combinational Gate

In this section, we explain how we can construct the proposed energy recovery logic combinational gate. A general structure for ERL-based combinational gates is shown in Figure 12 for n inputs.
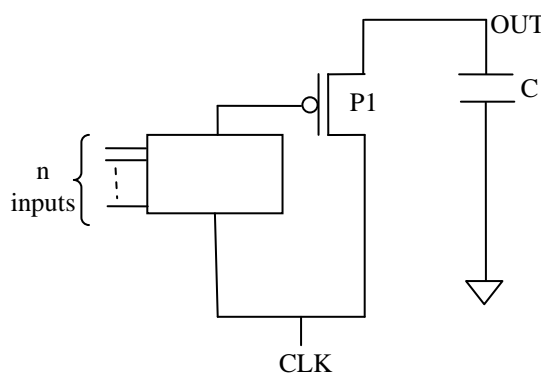

Figure 12: Proposed ERL Combinational Gate

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1) First step, find the complement of Boolean function F i.e.   .
2) Then it (complement of Boolean function F) is implemented by nMOS transistors, also called n-tree.
By these two steps we can implement all basic ERL combinational logic gate and logic circuit.

III.   CONCLUSION

Adiabatic logics are highly helpful for implementation of power efficient designs. These logics are alternative technique for circuit design as compared to pipelining and other techniques that requires high circuit complexity. Energy recovery logics has successfully used for fundamental VLSI blocks such as adder, subtractor and other arithmetic circuits. Further from simulation results, it may be observed that proposed ERL circuits offers improved performance in power dissipation with reduction in circuit complexity.

Hence, it is concluded that the proposed design circuit will provide a platform for designing high performance and low power digital circuits such as digital signal processors, adders and multiplexers. One of the disadvantages of energy logic circuits is that the speed of operation is reduced with reduction in power dissipation.

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